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Study on Various Converter Topologies For Power Factor Improvement In SMPS

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Abstract:*Due to severe power shortage, the power suppliers are unable to meet the power demand and are forced to purchase it from other states. One method to overcome power shortage, is by improving power factor at the customer side, thereby the energy wasted by various equipment due to low power factor can be reduced. Nowadays personal computers (PCs) are an inevitable part of our day to day activities for which Switched Mode Power Supplies (SMPS) is an integral part. The problem associated with multipleoutput SMPS is its very poor power factor and voltage regulation and the high totalharmonic distortion, which violate the limits of harmonic emissions set by internationalpower quality standards. Hence to improve the power factor and thereby the powerquality a power factor corrected (PFC) converter is used which is ableto reduce the 100 Hz ripple in its output. This improved output is fed to the secondstage isolated converter (SMPS). Control of the Power factor correcting unit as wellas the isolated converter is using a PI controller.This can be used in various server power systems, telecommunication systems andmobile applications. In this paper a study of various types of converter for Power factor improvement in SMPS is performed.*

Keywords: *Multiple Output SMPS,Personnal computer,Sheppard Taylor Converter, Bridgeless Buck-Boost Converter, Zeta Converter.*

I. Introduction

Increasing awareness related to harmonic pollution has enticed the design of improved power quality (PQ) switched mode power supplies (SMPSs) in today's scenario. Conventional PC's use linear power supply which deteriorates the PQ due to harmonic pollution,high transformer losses and low power factor at the point of utility interface. This lowers the efficiency and places stress on various circuit components thus lowering their shelf-life. Currently, we focus on green energy and PQ improvement. This is especially pertinent in industrial scenarios where a large number of electronic devices are used which are vulnerable to PQ related issues. This is becoming relevant even in a home scenario as a huge procreation of electronic devices (e.g., laptops, tablets, cell-phones, televisions) is found even in home environment. In fact, now several standards have been set which limits the maximum current distortion that is permissible in power supplies. Because of this, improved power quality SMPSs are becoming more prevalent these days which also provide a solution to the constraints of low cost, compact size and moderate stress levels across the components. Personal computers (PCs) utilize such SMPSs to convert single-phase ac voltage into multiple dc voltages of desired magnitudes associated with a high frequency link. The unrestrained charging and discharging of the large capacitor after the diode bridge in conventional SMPS leads to highly distorted, periodically dense supply current, high crest factor (CF) and low power factor with reduced lifetime. Therefore, it is necessary to incorporate a power factor correction (PFC) converter at the front-end of an SMPS to attain improved PQ and to regulate the multiple dc voltages even at varying supply voltages and loading conditions. The PFC circuits are integrated in these SMPSs in singlestage or in two stages. Single stage SMPS for PCs are less popular because of inadequate output voltage regulation, excessive component stress, high output capacitance value and complex control. However, there is only one conversion stage improving the efficiency and number of components are less as compared to two stage SMPS. On the contrary, the two stage SMPS offers regulated dc output voltage, improved input PQ and a reduction in second order harmonic resulting in reduced value of output filter capacitors; it also offers fast dynamic response. Hence, the choice of number of conversion stages is a tradeoff between the above mentioned performance criteria. Usually, a boost converter is preferred for the PFC stage in most of the two stage SMPSsystems,although the output dc voltage range is restricted in this case. To expand the output voltage control range even with supply voltage variations, buck-boost converters seem to be a very viable option especially for PC power supplies. The SheppardTaylor (S-T) buck-boost converter is chosen here for PFC because it can provide both buck and boost operation with high level of PQ, excellent output voltage regulation and low device stress. Although, the component count is increased when compared to the other buck-boost converters, the current stresses of the high frequency synchronized switches are low and the control circuitry is very simple. The regulated output from the PFC S-T converter is connected to an isolated halfbridgeVSI

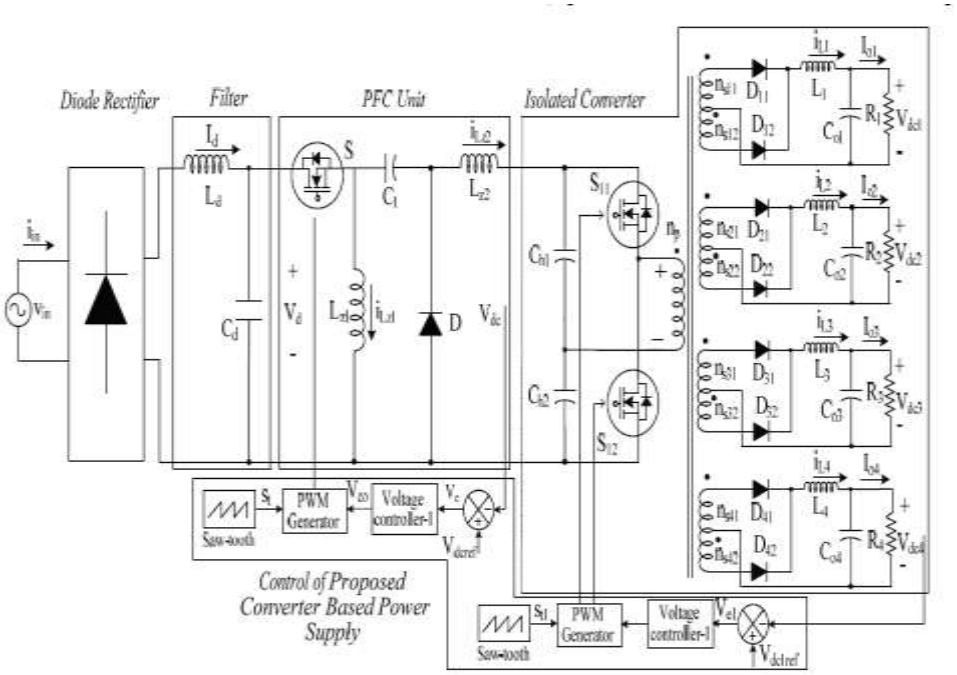
(Voltage Source Inverter) based dc-dc converter to provide multiple dc outputs. In the present era, personal computers (PCs) have become a part of our daily life. Apersonal computer power supply normally requires multiple number of DC-DC converters for multiple, isolated and regulated output with improved power quality. Hencethe complexity and cost of the system will be high. Now a days, switching converters have become very popular due to recent advances in semiconductor technology.Switching devices are available with very high switching speeds and very high power handling capabilities. It is possible to design switching mode power supplies with efficiency greater than 90 with low cost, relatively small size and light weight. In thisswitching converters, power semiconductor devices are used to operate either on-stateor the off state. Since either state will lead to low switching voltage or low switchingcurrent voltage conversion can be done with higher efficiency using a switching regulator. So now a days SMPS is used as an integrated part of personal computers. Itcan convert AC voltage in to multiple output dc voltages to impart power to differentparts of the PC. It contains a Diode Bridge rectifier (DBR) with a capacitor filterfollowed by an isolated DC-DC converter to achieve multiple DC output voltages of different ratings. The uncontrolled charging and discharging of the capacitor result in ahighly distorted, high crest factor, periodically dense input current at the single phaseac mains; this violates the limits of international Power Quality (PQ) standards suchas IEC 610003-2. Further, the neutral current in the distribution system increases ifthese PCs are used in large numbers which creates serious problems like overloadingthe neutral conductor, noise, de-rating of the transformer, voltage distortion etc. Sothat to solve this problem, improved power quality SMPS that are working with unitypower factor are extensively being researched A variety of circuit topologies have been developed for the Power Factor Correction(PFC) applications. The features of the good power factor correction circuit are asfollows: a well-regulated output voltage, isolation between input AC mains and outputDC mains, a sinusoidal line current with minimum THD. The various converter topologies are discussed below:

II. Zeta Converter For Power Factor Improvement

Fig1 shows the system configuration of a PFC Zeta converter based multi-output SMPS topology. At the input, a DBR with filter is connected to a nonisolated Zeta converter. It consists of two inductors Lz1and Lz2, one intermediate capacitor C1, one high frequency switch S and one diode D. This PFC converter regulates the output dc voltage and draws a sinusoidal current from the ac mains at unity PF. The output dc voltage is regulated using a Proportional-Integral (PI) voltage controller. The regulated output dc voltage is connected to an isolated converter for achieving multiple dc voltages at the output. The isolated converter consists of two equal valued input capacitors, two switches, one High Frequency Transformer (HFT) and filters. The filters are usedin each output winding to reduce the output voltage and current ripples. Only one of the output voltages is directly sensed and the other output voltages are controlled by the duty cycle of the isolated converter. The winding that is selected for control action is of the largest power rating among all the outputs. Further, to reduce the component stresses, the isolated converter is designed in CCM. Another voltage PI controller is used here to regulate the output voltage. The Operation principle of the proposed system is explained below.

2.1 Zeta Converter

Zeta converter exhibits two different modes as follows: Mode1: The first mode is obtained when the switch is ON (closed) and instantaneously, the diode D is OFF. During this period, the current through the inductor L1 and L2 are drawn from the voltage source Vs. This mode is the charging mode. Mode2: The second mode of operation starts when the switch is OFF and the diode D is ON position. This stage or mode of operation is known as the discharging mode since all the energy stored in L2 is now transferred to the load R.



. **Fig1:** Power factor Corrected zeta converter based SMPS

2.2 Isolated Converter

The operation of the isolated half-bridge converter working in CCM is described in two states during one half of the switching cycle where the upper switch is involved. In the second half of one switching cycle, the same procedure repeats with the involvement of the lower switch.

1. Inductor Charging

The output voltage of the PFC Zeta converter is connected to one end of the primary winding of the HFT through switch S_{11}. Diodes D_1, D_3, D_5, D_7start conducting. So, the output currents,i_{L01} ,i_{L02} ,$i_{L03}$and i_{L04}in inductors increase. When the inductor current reaches its maximum value, S_{11} is turned off.

2. Inductor Discharging

The output inductor current in each secondary winding freewheels through corresponding diodes (,$D_1 - D_8$). The current in each winding cancels the flux until the voltages across all windings are reduced to zero. The same inductor charging and discharging take place in the next half of the switching cycle when the lower switch turns on and then turned off subsequently.

III. Sheppard Taylor Converter For Pf Improvement

The schematic diagram of an SMPS for a PC is illustrated in Fig.2, which utilizes a PFC S-T converter. This converter offers both input PQ improvement and stiff output voltage regulation. It has two high frequency synchronized switches $S_1$and S_2 four high frequency diodes, D_1, D_2, D_3, D_4two inductorsL_1 and L_2 one intermediate capacitor C_{in},. The intermediate capacitor acts as a link that transfers energy from input to output in a controlled manner. The output inductor of S-T converter is designed in Discontinuous Conduction Mode (DCM) to achieve inherent PFC. Both high frequency switches are turned on and off in a synchronized manner. The dc output is further linked to a half bridge VSI, multiple output high frequency transformer (HFT), rectifying diodes and filters. Half bridge VSI has two high frequency switches $S_{h1}$and $S_{h2}$and two input capacitors$C_{11}$and C_{12}. HFT consists of one primary winding and four secondary windings to provide four different dc voltages $V_{01,}V_{02}, V_{03}$and V_{04} to various parts of the computer. The switching signals for the inverter switching are generated through two current control loops in d-q-0 co-ordinate system. The inverter operates in conventional controller mode only provided that Switch-2 is in OFF position. V_d=0 hence, Qref is only proportional to I_d which sets the reference I_{dref} for the upper control loop involving PI1. Meanwhile, the quadrature axis component I_q is used for DC link voltage control through two PI controllers (PI-2 and PI-3) according to the set point voltage provided by the MPPT and as well as injects all the available real power P to the network. To generate the proper IGBT switching signals, the d-q components (md and mq) of the

modulating signal are converted into three phase sinusoidal modulating signals and compared with a high frequency (5 kHz) fixed magnitude triangular wave or carrier signal.

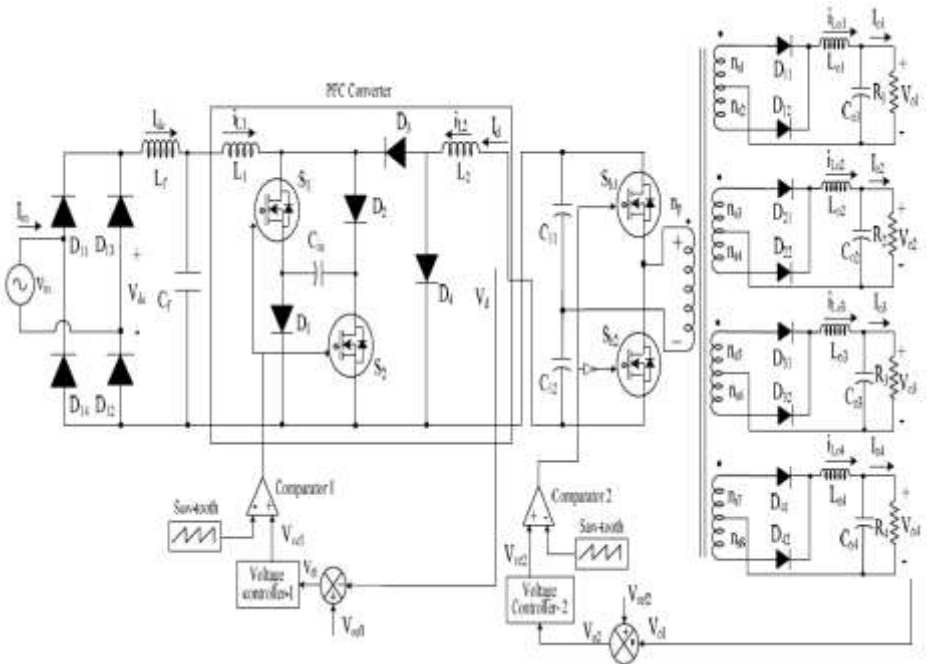
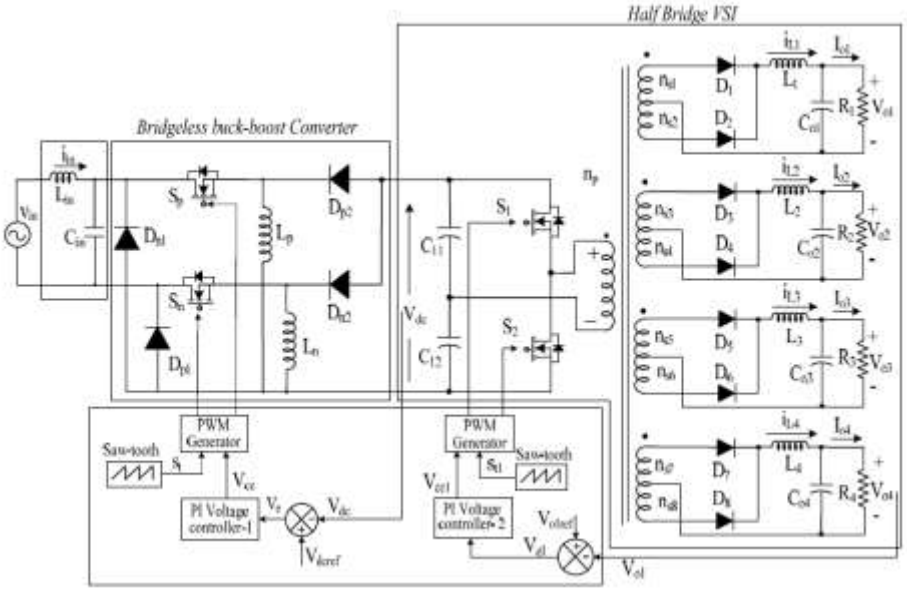


Fig 2: Schematic configuration of PFC Sheppard-Taylor based SMPS system

In the PCC voltage control mode of operation, the PCC voltage is controlled through reactive power exchange between the DG inverter and the grid. The conventional Q control channel is replaced by the PCC voltage controller, simply by switching the Switch-1 to the position A. The rest of the controller remains unchanged. The upper current control loop regulate the PCC voltage where the lower current control loop is used for DC voltage control. The amount of reactive power flow from the inverter to the grid depends on set point voltage at PCC. The parameters of the PCC voltage controller are tuned by systematic trial and error method to achieve the fastest step response, least settling time and a maximum overshoot of 10-15%.

IV. Bridgeless Buck Boost Converter For Pf Improvement

The system configuration of the proposed multiple output SMPS is shown in Fig. 3. Single-phase ac supply is fed to two buck-boost converters through an inductor-capacitor (L_{in} and C_{in}) filter to eliminate the high frequency ripples. The upper buckboost converter that conducts during the positive half cycle of the ac supply consists of one high frequency switch S_p, inductor L_p and two diodes D_{p1} and D_{p2}. Similarly, the lower buck-boost converter that operates during the negative halfcycle consists of one high frequency switch S_n, inductor L_n and two diodes $D_{n1}$and D_{n2}. Both inductors $L_p$and L_n of buckboost converters are designed in DCM to obtain inherent PFC at the input ac mains. The input capacitor of the half-bridge VSI acts as the filter at the output of the buck-boost converter. The voltage and current stresses on the switches of the buckboost converters are evaluated to estimate the switch rating and heat sink design.



The output dc voltage of the buck-boost converter is regulated by using closed loop control. The regulated dc output voltage of buck-boost converter is fed to the half-bridge VSI for obtaining multiple dc voltages. The half-bridge VSI consists of two input capacitors $C_{11}$and C_{12}, two high frequency switches$S_1$and S_2, one multiple output High Frequency Transformer (HFT). The HFT is having one primary winding and four secondary windings which are connected in centre tapped configuration to reduce the losses. At the secondary side of the HFT, filter inductors L_1, L_2, L_3, L_4 and capacitors C_{01}, C_{02}, C_{03}, C_{04} are connected to each winding to reduce the current and voltage ripples respectively. The output voltages are regulated by using closed loop control of one of the output voltages. The highest rated dc voltage is sensed for this purpose. The other three outputs are controlled through duty ratio control of the half bridge VSI because a common core is used for all the other secondary windings of the HFT with proper winding arrangements. The effect of varying input voltages and loads is studied to reveal the improved performance of proposed bridgeless converter based multiple output SMPS.

V. Conclusion

A DCM operated front end PFC converter cascaded with a multiple output isolated converter has been used for the design of an SMPS for PCs. It has been designed and developed for input power quality improvement and output voltage regulation. All the dc output voltages are regulated by controlling only one output voltage. The proposed power supply is able to mitigate power quality problems that are present in the conventional SMPS systems. Based on these results, it is concluded that the proposed SMPS configuration in PCs is expected to yield improved THD of ac mains current with almost unity PF under wide range of input voltages and loads.

A PFC S-T converter based SMPS system has been proposed for improving PQ at the front end of a power supply for personal computers. Constant dc voltage has been achieved by using PFC S-T converter which results in less switching device stress and excellent output voltage regulation at the output**.** A bridgeless converter based multiple output SMPS has been designed, modeled, simulated and implemented in hardware to demonstrate its capability to improve the power quality at the utility interface. The output dc voltage of the first stage buck-boost converter has been maintained constant, independent of the changes in the input voltage and the load and it is operated in DCM to achieve inherent PFC at the single phase ac mains.

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